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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,501	01/12/2004	Yun-Woo Lee	SEC.1091	8300

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/754,501	LEE ET AL.
	Examiner	Art Unit
	Long Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 3-7* is/are allowed.

6)☒ Claim(s) *12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Tsuda (JP 5-315931).

With respect to claim 12, Figure 1 of the Tsuda reference discloses a level shifter circuit, comprising: a first power (Vcc); a second power (Vdd); an input circuit (2-3); an input signal (T); an output circuit (QP1, Q1-Q4, QN1, 4); and a detection circuit (10, also see Figure 4 and paragraph [0014] of the translation); wherein the output circuit output circuit (QP1, Q1-Q4, QN1, 4) comprises an inverter (4) having an input that is grounded in response to the interruption detected by the detection circuit (because QN1 is ON so inverter 4 having its input connected to ground). Note that for broadest reasonable interpretation, when the power supply voltage VCC rises abnormally then it is considered that the power supply voltage VCC is interrupted since the normal voltage has been interrupted.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Konishi (USP 6,373,285) in view of Weste et al. (Principles of CMOS VLSI Design: A Systems Perspective, Addison-Wesley Publishing Company, 1993, second edition, section 10.5.4, pages 408-411).

With respect to claim 12, Figure 1 of the Konishi reference discloses a level shifter circuit, comprising: a first power (70); a second power (80); an input circuit (1); an input signal (10); an output circuit (2); and a detection circuit (3) for detection an interruption in the supply of the first voltage level by the first power supply node, and it is seen in the operation of the circuitry in Figure 1 of the Konishi reference that the interruption occurs during a power down operation mode (see abstract). Figure 1 of the Konishi reference does not disclose that the output circuit (2) includes an inverter having an input that is grounded in response to the interruption detected by the detection circuit. However, the Weste et al. reference discloses that an output buffer (chain of inverter) is desired to drive large load for reducing the time delay (see section 4.6.3, pages 229-231). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the level shifter circuit in Figure 1 of the Konishi reference by providing an output buffer (chain of inverters) to the output terminal 27 for the purpose of reducing the time delay when driving a large load such as long busses or downstream circuitry. Thus this modification/combination meets all the limitations of claim 13 that the output circuit including an inverter (the inverter of the output buffer coupled to terminal 27) having an input that is grounded in response to the interruption detected by the detection circuit (i.e., when the detection circuit 3 detects an interruption in the first power supply voltage 70, then signal 39 = Hi to turn on transistor 25 so the signal at terminal 27 is grounded, and thus the input of the inverter (of the output buffer) connected to terminal 27 is grounded).

Allowable Subject Matter

5. Claims 1 and 3-7 are presently allowed because applicant incorporates the allowable subject matter of claim 2 into independent claim 1.

Response to Arguments

6. Applicant's arguments filed on 6/30/05 have been fully considered but they are not persuasive.

Applicant argues that the Tsuda reference does not detect an interruption in the supply of the first voltage. However, this argument is not persuasive because the Tsuda reference clearly discloses that the detection circuit (10, Figure 1) detects an abnormal rises of the first power supply voltage, and thus for broadest reasonable interpretation, an interruption in the supply of normal voltage of the first power supply is detected (i.e., the normal operation voltage of the circuitry is interrupted). Thus, circuit 10 in Figure 1 of Tsuda detects an interruption in the first power supply.

Note, for claim 13, the amended changed the scope of the claim, and the argument has been considered but is moot in view of the new ground rejection (103 rejection).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 18, 2005

LONG NGUYEN
PRIMARY EXAMINER